IN THE CLAIMS

Claims 1-21 (Canceled)

22. (New) A method of manufacturing a semiconductor device having a gate lead-out region and a MISFET-forming region, comprising the steps of:

forming a trench in said MISFET-forming region of a major surface of a semiconductor substrate;

forming a gate insulating film of a MISFET in said trench;

forming a conductive film over an entire area of said major surface of said substrate such that said trench is filled by said conductive film through said gate insulating film and such that said conductive film is formed over a gate lead-out region of said major surface of said substrate; and

selectively etching said conductive film to form a gate electrode in said trench and to form a gate lead-out electrode over said gate lead-out region such that said gate lead-out electrode is integrally formed with said gate electrode,

wherein the top surface of said gate electrode is lower than the top surface of said semiconductor substrate in said gate lead-out region.

23. (New) A method according to claim 22, wherein said conductive film is formed by a CVD method.

24. (New) A method according to claim 22, wherein before said selectively etching step, a surface of said conductive film is flattened.

25. (New) A method of manufacturing a semiconductor device, comprising the steps of:

forming a trench in a MISFET-forming region of a major surface of a semiconductor substrate such that said trench is not formed in a gate lead-out region of said major surface of said substrate;

forming a gate insulating film of a MISFET in said trench;

forming a conductive film over an entire major surface of said substrate such that said trench is filled by said conductive film through said gate insulating film and

such that said conductive film is formed over said gate lead-out region; and

selectively etching said conductive film to form a gate electrode in said trench and to form a gate lead-out electrode over said gate lead-out region such that said gate lead-out electrode is integrally formed with said gate electrode,

wherein the top surface of said gate electrode is lower than the top surface of said semiconductor substrate in said gate lead-out region.

26. (New) A method according to claim 25, wherein said conductive film is formed by a CVD method.

27. (New) A method according to claim 25, wherein before said selectively etching step, a surface of said conductive film is flattened.